REMARKS

This paper responds to the final Office Action mailed November 2, 1998 ("the Office Action"). Applicant respectfully requests reconsideration of the present application in light of the above amendments and the following remarks.

Claim amendments

Proposed amendments for claims 1, 8, 9 and 13 are presented herein. The amendments are proposed for the purpose of clarifying the claim language; not for purposes relating to patentablility over the prior art. As such, the amendments are believed to be proper for entry in this case.

Telephone interview

The undersigned discussed the present application with Examiner Kenneth Wells during a telephone interview on November 10, 1998. The Examiner's participation in the telephone interview is greatly appreciated. The claims of the present application and the cited prior art references in light thereof were discussed.

35 U.S.C. § 112

Section 1 of the Office Action noted that the rejection of claims 1, 8, 13 and 15 under 35 USC 112 has been overcome by the amendments and arguments presented in Applicant's Amendment filed on September 17, 1998. The Examiner's acknowledgment of this is appreciated.

35 U.S.C. § 103

Section 3 of the Office Action rejected claims 1-16 under 35 USC 103(a) as being unpatentable over U.S. Patent No. 4,636,907 to Howell ("Howell") or U.S. Patent No. 4,688,267 to Chown et al. ("Chown"). Applicant respectfully traverses these rejections.

A transistor that receives signals of a first level and delivers signals of a second level–

First, each of independent claims 1,8, 13 and 15 of the present application include a transistor that receives signals of a first level and delivers signals of a second level. Such transistors are commonly referred to as a "pass gate" transistor, because they pass, or transmit, digital data to various circuits on an integrated circuit. Neither Howell nor Chown disclose or suggest such an element.

Howell is directed to an arcless circuit interrupter for reducing the arc that occurs between separating contacts within a protected circuit, and does not teach or suggest the use of a pass gate transistor to receive signals of a first preselected voltage level and deliver signals of a second preselected voltage level. The purpose of the circuit disclosed in Howell is to "describe a circuit which completely eliminates the occurrence of an arc between separating contacts both under ordinary circuit conditions as well as upon the occurrence of an overload condition." Howell at col. 1, lines 54-58. Howell provides an "impedance circuit," which in the embodiment illustrated in Figure 3, includes an FET. A control circuit biases the impedance circuit normally on, allowing current to flow through the impedance circuit. When it is desired to interrupt the circuit current, bias is removed from the impedance circuit to increase the impedance thereof to divert the current through the current interrupter. Howell does not disclose "an apparatus for

converting signals" as claimed. Howell does not disclose a transistor that receives signals of a first level and delivers signals of a second level.

Chown discloses an optical receiver that includes an FET. Chown, however, does not disclose "an apparatus for converting signals" as claimed. As noted above, each claim of the present application includes a transistor that receives signals of a first level and *delivers signals* of a second level. In Chown, the source terminal of the FET is connected to ground. Thus, the output terminal, or source, is not for "delivering signals of the second preselected voltage level."

Applicant respectfully submits that Howell and Chown do not teach or suggest the transistor of independent claims 1, 8, 13 and 15; thus, these claims, and all the claims depending therefrom, are believed to be proper for allowance.

Enable or gate terminal coupled to voltage supply–

Further, independent claims 1, 8 and 13 each recite the enable or gate terminal of the transistor being coupled to a voltage source. Claim 13 specifically states that the voltage supply has a third preselected voltage level, and claim 1 and claim 9 (depending from claim 8) each additionally include a resistive element coupled between the enable or gate terminal and the voltage supply. Neither Howell nor Chown disclose or suggest these elements.

During the November 10, 1998, telephone interview, the Examiner agreed that the Howell and Chown references did not appear to disclose the element of the transistor gate being coupled to a voltage supply, and the Examiner invited Applicant to discuss this point in a response to the Office Action such as this.

The pass gate transistor of the present claims has its enable, or gate, terminal coupled to a voltage supply to continuously bias the transistor on and pass a portion of the voltage of the first

voltage level present at the input, or drain, terminals to the output, or source terminal. Nowhere in Howell or Chown is this claim element taught or suggested.

With regards to claims 6 and 7 (depending from claim 1) and 11 and 12 (depending from claim 8), Howell and Chown further do not teach or suggest coupling the enable, or gate, terminal to a resistive element that comprises a resistor or a transistor.

Since Howell and Chown do not teach or suggest the enable, or gate, terminal being coupled to a voltage supply, Applicant believes that independent claims 1, 8 and 13, as well as the claims depending therefrom, are proper for allowance.

Charging the gate to a fourth preselected voltage level –

Independent method claim 15 includes the following elements:

> charging a gate of a pass gate transistor to a third preselected voltage level to enable the pass gate transistor to pass at least a portion of the voltage level of the input signal to an output node;
>
> charging the gate of the pass gate transistor to a fourth preselected voltage level for a preselected period of time, said fourth preselected voltage level being greater than said third preselected level; and
>
> passing at least a portion of any AC component in said input signal to said output node.

Howell and Chown do not teach or suggest a method such as this. As discussed hereinabove, Howell and Chown do not recite devices or methods for converting and transmitting digital signals, as they are directed to an arcless circuit interrupter and an optical receiver, respectively.

Hence, they do not disclose the method of claim 15. While Howell and Chown disclose circuits containing an FET, they do not teach or suggest any of the claim elements reproduced above.

Particularly, claim 15 includes charging the gate to a third voltage level, and charging the gate to a fourth preselected voltage level that is higher than the third level, for a preselected period of time. Similarly, independent claim 13 includes a pass gate transistor having its gate coupled to a voltage supply having a third voltage level, and means for temporarily increasing the voltage level applied to the gate. Still further, claim 8 includes the element of a pump configured to temporarily increase the voltage level applied to the gate. Nowhere in Howell or Chown is there a disclosure or suggestion of temporarily increasing the bias applied to the gate of a pass gate transistor.

For these reasons, in addition to the reasons set forth above, Applicant believes that independent claims 8, 13 and 15, and the claims depending therefrom, are in proper form for allowance.

Buffer circuit –

Dependent claims 2 - 5 include the element of a buffer circuit coupled to receive signals from the transistor output terminal. Neither Howell nor Chown disclose or suggest a buffer circuit coupled to the output of the transistors disclosed therein. Thus, Applicant respectfully submits that neither Howell nor Chown can render claims 2 - 5 unpatentable. Moreover, as discussed above, Howell discloses an arcless circuit interrupter and Chown discloses an optical receiver. As the FETs disclosed in Howell and Chown are not provided for transmitting digital signals, there would be no reason to couple a buffer circuit to the output of the FETs disclosed in Howell and Chown.

For these reasons, in addition to the remarks set forth above regarding independent claim 1, Applicant respectfully submits that claims 2 - 5 are patentable over Howell and Chown.

CONCLUSION

In response to the last Office Action, Applicant has offered the above remarks in a genuine effort to advance this case towards issuance. These remarks are presented, in part, in response to the Examiner's invitation during the November 10, 1998, telephone interview to present such arguments regarding the claim elements in light of the cited prior art, and more specifically, to the absence of a teaching or suggestion in the prior art of coupling the pass gate transistor's gate terminal to a voltage supply. Based upon the above remarks, Applicant believes that the pending claims are all in proper form for allowance. Therefore, reconsideration of these claims is respectfully requested.

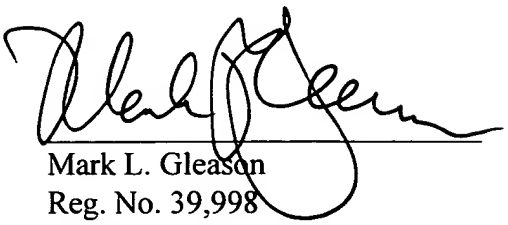
In the event that the Examiner does not believe that the amendments and remarks place all of the claims in proper form for allowance, the Examiner is requested to withdraw the final rejection entered in this case to allow Applicants to further address any concerns that the Examiner may have concerning the patentability of the claims in the present application.

If the Examiner believes that a telephone conference would be beneficial to advance this case towards allowance, he is strongly encouraged to telephone the undersigned at the number provided below.

It is believed that no fee is due; however, should any fees under 37 C.F.R. §§ 1.16 to 1.21 be required for any reason, the Assistant Commissioner is authorized to deduct said fees from Arnold White & Durkee Deposit Account No. 01-2508/INPA:035/GLE.

Respectfully submitted,

Date: 12/14/98

By: 

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